Aidan Prendergast

ASIC Design and AI Hardware Engineer

EDUCATION

Purdue University — West Lafayette, IN

M.S. Electrical and Computer Engineering — GPA 3.90/4.0 B.S. Electrical Engineering — GPA 3.92/4.0

SystemVerilog, C, CUDA, Assembly — ASIC Design, Microprocessor Design, GPU Architecture Questa, Design Compiler, Quartus, C++, Gem5 — NES Senior Design Project, Computer Architecture, ASIC Design Python, Octave, Neural Network Arch — SCALE, AI Hardware, ML, Generative Models Coursework Virtuoso, Transport Simulation Tools — VLSI, Semiconductor Devices, Research Work

Leadership, Mentorship, Communication, Technical Writing — Publications, Eagle Scout Award, Industry Positions

EXPERIENCE

Head Graduate Teaching Assistant — Purdue ECE ASIC Design Laboratory

- Instructing 150+ students per semester in hardware design and leading a team of 7 Grad TAs + 25 Undergrad TAs.
- Redeveloped course content, reinventing six teaching labs + retooling five advanced labs for clarity and impact.
- Introducing matrix compute content to expose students to current AI Hardware design needs and challenges.

Microelectronics Intern — L3Harris Technologies, Inc

- Advised and oversaw development on a Python database for optical field hardware selection and delivery. •
- Organized and documented pack-out procedures on mission-critical hardware for a 5-year top secret contract.

Chip Design Teaching Assistant — Purdue University STARS

- Identified need for, developed, and presented supplementary lectures for 75+ Digital Design Students.
- Directed two project teams in designing custom multichannel digital synthesizer integrated circuit modules.

Undergraduate Teaching Assistant — Purdue ECE ASIC and Digital Design Labs Jan 2022 — May 2024

- Reinforced SystemVerilog and digital design concepts and evaluated performance for over 600 students.
- Mentored fellow teaching assistants and facilitated hiring of 20+ TAs targeting team sustainability and longevity.
- Systems Engineering Intern Raytheon Intelligence and Space
 - Redeveloped RF engineering tools for military ATC system R&D, improving internal testing speeds by up to 20x.

PROFESSIONAL ORGANIZATIONS & PROJECTS

Team Lead and Compute Core Lead Engineer — Project Chronomancer

- Founded an Out-of-Order processor project team focused on RISC-V core design with advanced optimizations.
- Leading development of a SystemVerilog R10K processor and verification + benchmarking infrastructure.

Research Assistant for AI Hardware Development — Purdue SCALE

- Creating two AI Hardware course modules and two accelerator design lab assignments for the Undergrad level.
- Linking hardware and education experts to create high-impact, comprehensive introductory-level modules.

Team Lead and Hardware Design Engineer — Hardware-Emulated NES Senior Design Jan 2024 — May 2024

- Led a team of four to prototype in 4 months an FPGA-Based Nintendo capable of playing original cartridges. •
- Reverse-engineered and verified a proprietary video coprocessor and custom VGA translator in SystemVerilog.

Student Ambassador — Purdue ECE Ambassadors

Serving as a Student Representative, interfacing with donors and alumni, vetted three new department advisors.

PUBLICATIONS & AWARDS

- *Real-Time Generation of Hyperbolic Neuronal Spiking Patterns*. 1st Auth. https://ieeexplore.ieee.org/document/9870915.
- An organic synaptic circuit: towards flexible and biocompatible organic neuromorphic processing. • https://doi.org/10.1088/2634-4386/ac830c.
- 2023-2024 Undergraduate Service Award, Purdue University.

2023-2024 Senior Design Award, for the Hardware-Emulated NES Project. •

Eagle Scout, Boy Scouts of America Troop 60.

Awarded Dec 2024 Awarded Dec 2024 Awarded Dec 2018

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May 2024 — Aug 2024

May 2023 — Jul 2023

Nov 2024 — Present

Sept 2024 — Present

May 2024 — Present

Aug 2020 — Present

Anticipated Graduation May 2025

Graduated Cum Laude May 2024

May 2022 — Aug 2022

Jan 2022 — Present